SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 USC §119 to Korean Patent Application No. 10-2015-0079606, filed on Jun. 5, 2015 in the Korean Intellectual Property Office (KIPO), the contents of which are herein incorporated by reference in their entirety.

BACKGROUND

[0002] 1. Field

[0003] Example embodiments relate to a semiconductor device and/or a method of manufacturing the same. More particularly, example embodiments relate to a variable resistance memory devices and/or methods of manufacturing the same.

[0004] 2. Description of Related Art

[0005] As semiconductor devices are highly integrated, variable resistance memory devices having cross point array structures have been manufactured.

SUMMARY

[0006] Example embodiments relate to a semiconductor device including lower and upper patterns exactly aligned with each other.

[0007] Example embodiments relate to a method of manufacturing a semiconductor device including lower and upper patterns exactly aligned with each other.

[0008] According to example embodiments, a semiconductor device includes a substrate, a plurality of first conductive lines, a plurality of first structures, a first insulation pattern, a second insulation pattern, a variable resistance pattern, and a second electrode. The first conductive lines are on the substrate. The first conductive lines extend in a first direction. The first structures may be spaced apart from each other, and may be on the first conductive lines. The first structures include a switching pattern and a first electrode sequentially stacked. Top surfaces of the switching pattern and the first electrode are substantially coplanar with each other. The first insulation pattern is on the substrate. The first insulation pattern extends in the first direction between the first structures to fill a space between the first structures in a second direction that is substantially perpendicular to the first direction. The first insulation pattern has a first top surface that is higher than a top surface of the first structures. The second insulation pattern is on the substrate. The second insulation pattern extends in the second direction to fill a space between the first structures in the first direction. The second insulation pattern has a second top surface that is higher than a top surface of the first structures. The variable resistance pattern is on the first structure, and the variable resistance pattern fills an opening defined by the first and second insulation patterns. The second electrode is on the variable resistance pattern.

[0009] In example embodiments, the semiconductor device may further include a first spacer on upper sidewalls of the first insulation pattern above the first structure, and a second spacer on upper sidewalls of the second insulation pattern above the first structure.

[0010] In example embodiments, a bottom surface of the variable resistance pattern may be smaller than an area of the top surface of the first structures.

[0011] In example embodiments, the variable resistance pattern may be on a central upper surface of the first structure.

[0012] In example embodiments, a lower width of the variable resistance pattern may be less than an upper width of the variable resistance pattern.

[0013] In example embodiments, a top surface of the variable resistance pattern may be substantially coplanar with the first top surface of the first insulation pattern.

[0014] In example embodiments, the second electrode may extend in the second direction.

[0015] In example embodiments, the second top surface may be higher than the first top surface, and the second electrode may be between protruding portions of the second insulation patterns above the first insulation pattern.

[0016] In example embodiments, a top surface of the second electrode may be substantially coplanar with a top surface of the second insulation pattern or the top surface of the second electrode may be lower than the top surface of the second insulation pattern.

[0017] In example embodiments, the first and second insulation patterns may include substantially a same material.

[0018] In example embodiments, a second conductive pattern may be further formed on the second electrode, and the second conductive pattern may have a resistance lower than a resistance of the second electrode, and the second conductive pattern may extend in the second direction.

[0019] In example embodiments, a top surface of the second conductive pattern may be higher than the second top surface of the second insulation pattern.

[0020] In example embodiments, a top surface of the second electrode may be substantially coplanar with a top surface of the second insulation pattern or the top surface of the second electrode may be lower than the top surface of the second insulation pattern.

[0021] In example embodiments, the variable resistance pattern may include a chalcogenide-based material.

[0022] In example embodiments, the second electrode may have a pillar shape.

[0023] In example embodiments, the first and second top surfaces may be substantially coplanar with each other, and the second electrode may be on the variable resistance pattern in the opening defined by the first and second insulation patterns.

[0024] In example embodiments, a top surface of the second electrode may be substantially coplanar with a top surface of the second insulation pattern or the top surface of the second electrode may be lower than the top surface of the second insulation pattern.

[0025] In example embodiments, an upper width in the second direction of the first conductive line may be substantially the same as a lower width in the second direction of the first structure.

[0026] According to example embodiments, a semiconductor device includes a substrate, a plurality of first conductive lines, a plurality of first structures, a first insulation pattern, a second insulation pattern, a first spacer, a second spacer, a variable resistance pattern, and a second electrode. The first conductive lines are on the substrate and the first conductive lines extend in a first direction. The first struc-